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Letter

A tunable organic inverter based on groove patterned pentacene thin film transistors using soft-contact lamination

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ABSTRACT

Organic zero drive load inverters based on pentacene thin film transistors with periodic groove patterned dielectrics are fabricated using nanoimprinting and soft-contact lamination methods. Depletion mode transistor behavior is achieved when the current direction is parallel to groove direction and enhancement mode transistor behavior is achieved when the directions are crossed. An organic inverter is created after connecting two soft-contact laminated transistors. The electrical performance of the drive transistor can be varied and the organic inverter is tunable. This is done by utilizing a PDMS stamp with the source–drain electrode and changing the angle between the current direction and groove direction. The gain and symmetry of the VTC is improved by using an enhancement mode transistor where the source–drain electrode formed by thermal evaporation instead of being a soft contact-laminated device.

1. Introduction

With the increasing requirements for new functional electronic products, soft, flexible organic electronics have been extensively studied looking to improve upon traditional inorganic silicon techniques [1,2]. Inverters (logic doors) are elementary components for electrical circuits and are heavily used in those traditional techniques. Recently, organic inverters have been considered as one of the key elements in organic flexible circuits and have drawn more attention because they are flexible and economic to produce. Complementary circuits composed of both p-type and n-type transistors are typically used in silicon technology. However, in organic electronic circuits, organic inverters with only two p-type organic transistors also have been studied and accomplished by many research groups because of poor performance and instability in air of n-type organic transistors [3–6].

Among various organic inverters with two p-type transistors, a zero drive load inverter composed of both depletion mode transistor (loader) and enhancement mode transistor (driver) has been widely studied [7]. In a zero drive load inverter, as shown in Fig. 1(a), the source electrode of loader is connected to the gate electrode and the output voltage (V_{out}) is automatically obtained by the input voltage (V_{in}) since the current in the two transistors should be same. In fabrication of a zero drive load inverter, it is important to realize a large separation between source–drain current transfer curves (CTCs) of the driver and loader. Varying the ratio between the channel width and length (W/L) in the driver and loader is a simple and common method. Furthermore, changing channel thickness, utilizing different gate dielectrics, UV illumination and using dual gates are efficient methods for fabricating inverters [3–6]. Tuning of threshold voltages (V_{th}) can also be used for fabricating zero drive load inverters [8]. In previous work, the characteristics of pentacene thin film transistors with periodic groove patterned poly(methyl methacrylate) (PMMA) dielectrics have been studied [9]. When the angle between the source–drain current (I_{sd}) direction and groove direction increases from 0° to 90° by laminating with polydimethylsiloxane (PDMS) stamp [10–12], the current output and mobility of the charge carrier

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decreases with a negative shift in threshold voltage. Coincidently, these electrical phenomena including separation of the transfer curves and shift of threshold voltage are basic requirements for establishing a zero drive load inverter, therefore, adopting transistors with nano-groove patterned dielectrics combined with flexible stamps supplies us alternative methods for fabricating novel tunable organic inverters. Compared with known methods for making zero drive load inverters [3–6], it is possible not only to produce a zero drive load inverter, but also to tune the voltage transfer curves (VTCs) in one inverter by laminating it with a soft PDMS stamp and then changing the angle between the I_{sd} direction and groove direction without any input variation.

In this work, a VTC tunable zero drive load inverter is introduced by using pentacene thin film transistors with groove patterned PMMA dielectrics with soft-contact lamination from a PDMS stamp. The electrical performance of an inverter can be varied by utilizing the PDMS stamp with an Au electrode and changing the angle between the I_{sd} direction and groove direction.

2. Experimental

The driver and loader are connected as shown in Fig. 1(a) and the structures of the driver and loader are illustrated in Fig. 1(b). Indium tin oxide (ITO) on glass substrate is used as the gate electrode and patterned by photolithography and a wet etching process. It is then cleaned with detergent, deionized water, and with sonication in trichloroethylene, isopropyl alcohol and acetone. The PMMA thin film (10 wt.% in toluene) used as the gate dielectric is spin coated onto the ITO electrodes for 30 s at a rate of 3000 rpm and is annealed on a hot plate at 130 °C for 1 h. For nanoimprinting on the PMMA film, a UV curable poly(urethaneacrylate) (PUA) mold is prepared [13]. This

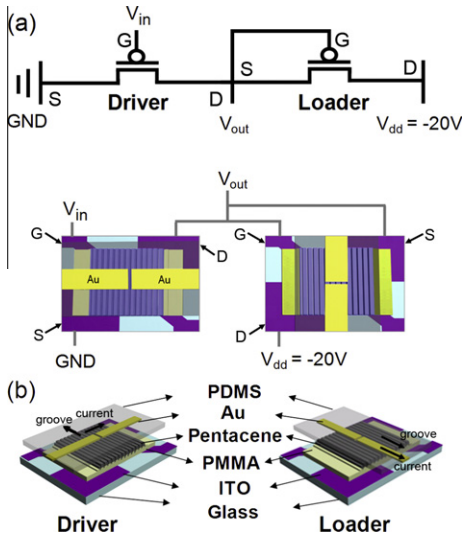

Fig. 1. Schematic illustrations of (a) circuit diagram of a zero drive load inverter, and (b) structures of driver (enhancement mode transistor) and loader (depletion mode transistor). S, D, and G are abbreviations for source, drain and gate electrode, respectively. The arrows on PDMS molds indicate directions of grooves and currents.

PUA mold with periodic, 120 nm high and 70 nm wide, line-and-space patterns are replicated from a silicon master and it is treated with monoglycidyl ether terminated PDMS to lower the surface energy [14]. The PMMA film is then pressed in the PUA mold under a pressure of 2.5 MPa at 130 °C for 5 min and the mold is demolded after cooling down to room temperature. Pentacene film (70 nm) is thermally evaporated onto the PMMA layer at a rate of 1 Å s^{-1} under vacuum condition (<5 × 10^{-6} Torr). For soft-contact lamination, an elastomeric flat PDMS stamp is cured at 60 °C for 24 h with a curing agent (Sylgard 184, Dow Corning), an Au source–drain electrode with a channel length of 120 μm and a width of 2500 μm is thermally evaporated onto the PDMS stamp through a shadow mask. This PDMS stamp with Au electrodes is brought into contact with the pentacene film. A pentacene transistor with a non-patterned PMMA dielectric is also used for improving the characteristics of the inverter and this device is known as the 'evaporated device (D_{evap})' in this work. In the evaporated device, flat PMMA film on ITO patterned glass is used and the Au source–drain electrode is directly evaporated onto the pentacene film instead of the PDMS stamp. Zero drive load inverters are fabricated by connecting two pentacene transistors with electric wires and the characteristics of the devices are measured by a semiconductor parameter analyzer (4200-SCS, keithley).

3. Results and discussion

The CTCs of both soft-contact laminated transistors and the evaporated devices are shown in Fig. 2(a). In the soft-contact laminated device with grooves on the PMMA dielectric, the output current increases gradually when the angle between the I_{sd} and groove direction decreases from 90° to 0° as shown in Fig. 2. The charge carrier mobility also increases from 0.05 to 0.25 $cm^2 V^{-1} s^{-1}$, whereas the mobility of the evaporated device is 0.1 $cm^2 V^{-1} s^{-1}$.

In addition, the threshold voltage (V_{th}) is shifted from −23.33 to −10 V in the soft-contact laminated transistors with patterned dielectrics when the angle decreases due to the variation of the capacitance and electric field along the current direction [9]. Interestingly, this stepped shift by angle variation is similar to the result achieved by changing the W/L ratio in the transistors when fabricating a zero drive load inverter. Consequently, a '0° device' where the I_{sd} is parallel to groove direction can be used as a loader and is abbreviated to 'L_0' in this work. Soft-contact laminated devices which have different crossed angles (30°, 45°, 70° and 90°) also can be used as drivers and are abbreviated to 'D_{30}', 'D_{45}', 'D_{70}' and 'D_{90}', respectively. Four different zero drive load inverters are fabricated by connecting a driver and loader with electric wires and their types are denoted by 'D_{30}–L_0', 'D_{45}–L_0', 'D_{70}–L_0', and 'D_{90}–L_0'. Under an input voltage from 10 to −30 V, the VTCs are obtained as shown in Fig. 2(b). According to the results in Fig. 2(b), an increase of angle in the driver causes the separation of the CTCs between the driver and loader to become larger and the VTC is shifted in a negative direction when the angle in the driver is changed from 30° to 90°.

If CTCs separation between the driver and loader becomes larger, causing the loader (depletion mode) to show

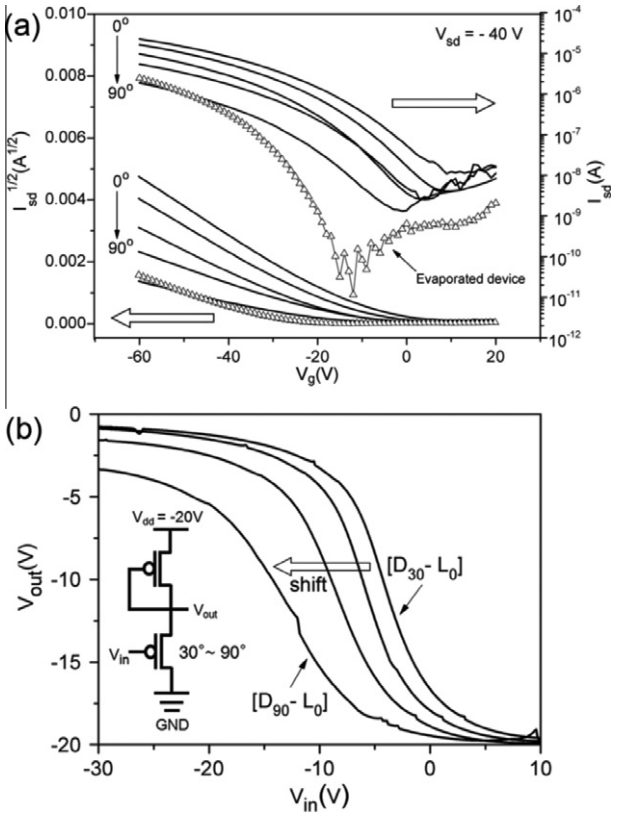

Fig. 2. (a) Current transfer curves of soft-contact laminated devices with different crossed angles (0°, 30°, 45°, 70° and 90°) and evaporated device. (b) The VTCs of zero drive load inverters consist of two soft-contact laminated devices with patterned PMMA dielectrics. Device with crossed angle of 0° is used as a loader and others with crossed angles of 30°, 45°, 70° and 90° are used as drivers.

a better turn-on state (higher source–drain current), when input voltage of the inverter is 0 V, the loader can supply a higher current than the driver. However, the output voltage, which comes from the gate electrode of the loader, would be pulled down to V_{dd} to decrease the source–drain voltage (V_{sd}) of the loader since the current in the two transistors should be same. On the other hand, V_{out} would not be instantly pulled down to V_{dd}, if the separation of the CTCs between the driver and loader is not large enough. That is, at certain V_{in}, a larger separation of VTCs between the driver and loader leads to lower (or a more negative) V_{out}, whereas a smaller separation leads to higher (or a less negative) V_{out}.

The separation of logical levels, which means the difference between on and off state of an inverter, of the four inverters are all around 15 V, which is within the range of the input voltage (0 V ~ −20 V), and the maximum gains, defined as $|dV_{out}/dV_{in}|_{max}$, are approximately 2.5 as shown in Fig. 2(b). A full swing can reach almost 19 V when the V_{in} sweep range is extended from 10 to −30 V, however, this is not consistent with V_{in} range. The full swing is large enough, but the logical separation is limited to only 15 V due to the inconsistency between V_{out} and V_{in}.

As shown in Fig. 2(a), the separation of CTCs between the evaporated and soft-contact laminated devices is large and this may lead to a proper operating range for the inverters at zero gate bias since a larger separation of CTCs between the driver and loader leads to lower (or more negative) V_{out}. Moreover, the evaporated device exhibits lower off-current than the soft-contact laminated device in our system and this is attributed to different source–drain contact resistances in these two different devices [11]. The evaporated device will be used as a driver in the inverter for increasing gain because of its relatively lower off current.

In general, the maximum gain (A_{max}) in the inverter is given by [7]:

$$A_{max} \approx k \frac{\frac{\partial I_{sd}}{\partial V_g}\big|_{v_g=0, V_{sd}=V_{sdH}}}{I_{sd}\big|_{v_g=0, V_{sd}=V_{sdH}} - I_{sd}\big|_{V_g=0, V_{sd}=V_{sdL}}} \quad (1)$$

where V_g is input voltage, I_{sd} is source–drain current of the driver, V_{sd} is source–drain voltage of the driver, V_{sdH} and V_{sdL} are logical high and logical low, and $k = V_{sdL} - V_{sdH}$ in this work. According to Eq. (1), the gain decreases when the conductivity of a bulk semiconductor without field effect increases because the current flow in a bulk semiconductor increases I_{sd} without changing the transconductance $\left(\frac{\partial I_{sd}}{\partial V_g}\right)$ [7]. Therefore, the conductivity of a bulk semiconductor is reduced by decreasing the off-current of I_{sd} for increasing the maximum gain and the evaporated device is adopted as the driver of the tunable inverter.

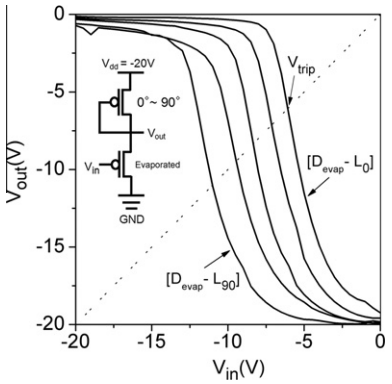

Fig. 3. The VTCs of inverters consist of evaporated device without nanogrooves and soft-contact laminated devices with patterned PMMA dielectrics. Evaporated device is used as a driver and soft-contact laminated devices with angles of 0°, 30°, 45°, 70° and 90° are used as loaders.

With an angle variation from 90° to 0° in the soft-contact laminated transistor, the CTCs separation between the evaporated device and soft-contact laminated device gradually increases as shown in Fig. 2(a). This is reflected in the VTCs of the different inverters, ('D_{evap}–L_0', 'D_{evap}–L_{30}', 'D_{evap}–L_{45}', 'D_{evap}–L_{70}', and 'D_{evap}–L_{90}'), and is represented by a negative shift and leads to a consistent V_{in} and V_{out} range as shown in Fig. 3. As a result, their logical separations are all over 19 V, and the maximum gain increases to 5.6. Symmetry with respect to the trip point (V_{trip}) gets better with the negative shifting of VTC. Inverters where an evaporated device is connected to a soft-contact laminated device with angle of 0° or 30° show a V_{trip} of −11 and −9.3 V, respectively, revealing better noise margins than other inverters with angles of 45°, 70° and 90°.

4. Conclusions

In conclusion, tunable organic zero drive load inverters based on pentacene thin film transistors with periodic groove patterned PMMA dielectrics are fabricated without changing the W/L ratio of the electrodes. A depletion mode transistor is produced when the current direction is parallel to the groove direction and an enhancement mode transistor is produced when the directions are crossed. A separation of the CTCs is achieved when the angle between the current and groove directions varies, tunable voltage transfer performance of the inverters can be realized by using a soft-contact PDMS stamp with the source–drain electrode. The gain and symmetry of the VTCs are improved when the device whose source–drain electrode is formed by thermal evaporation is used as the driver instead of the soft-contact laminated driver. Unconventional fabrication methods such as nanoimprinting and soft-contact lamination are efficient and economical methods for producing organic electronics and these techniques could also be adopted in other polymer dielectrics for wider applications. A series of experiments with other polymer dielectrics are now in progress to improve their performance and operation at low voltage.

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References

[1] G.H. Gelinck, H.E.A. Huitema, E.V. Veenendaal, E. Cantatore, L. Schrijnemakers, J.B.P.H. Van der putten, T.C.T. Geuns, M. Beenhakkers, J.B. Giesbers, B. Huisman, E.J. Meijer, E. Benito, F.J. Touwslager, A.W. Marsman, B.J.E. Van rens, D.M. De leeuw, Nat. Mat. 3 (2006) 106.
[2] F. Eder, H. Klauk, M. Halik, U. Zschieschang, G. Schmid, C. Dehm, Appl. Phys. Lett. 84 (2004) 2673.
[3] S.J. Mun, K. Lee, K.H. Lee, M.S. Oh, S. Im, Org. Electron. 11 (2010) 169.
[4] C. Baek, S. Seo, Appl. Phys. Lett. 94 (2009) 153305.
[5] J.M. Choi, J.H. Kim, S. Im, Appl. Phys. Lett. 91 (2007) 083504.
[6] J.B. Koo, C.H. Ku, J.W. Lim, S.H. Kim, Org. Electron. 8 (2007) 552.
[7] E. Cantatore, E.J. Meijer, Solid-State Circuits Conference ESSCIRC'03, Proceedings of the 29th European 2003, p. 29.
[8] M. Marchl, M. Edler, A. Haase, A. Fian, G. Trimmel, T. Griesser, B. Stadlober, E. Zojer, Adv. Mater. 22 (2010) 5361.
[9] Q. Sun, J.H. Kim, J.H. Park, S. Seo, Appl. Phys. Lett. 96 (2010) 103301.
[10] T.W. Lee, J. Zaumseil, Z. Bao, J.W.P. Hsu, J.A. Rogers, Proc. Natl. Acad. Sci. USA 101 (2004) 429.
[11] J. Zaumseil, K.W. Baldwin, J.A. Rogers, J. Appl. Phys. 93 (2003) 6117.
[12] J. Zaumseil, T. Someya, Z. Bao, Y.L. Loo, R. Cirelli, J.A. Rogers, Appl. Phys. Lett. 82 (2003) 793.
[13] S.J. Choi, P.J. Yoo, S.J. Baek, T.W. Kim, H.H. Lee, J. Am. Chem. Soc. 126 (2004) 7744.
[14] M.J. Lee, N.Y. Lee, J.R. Lim, J.B. Kim, M. Kim, H.K. Baik, Y.S. Kim, Adv. Mater. 18 (2006) 3115.